

x86 Disassembler Internals

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• Who am I?

Richard Johnson Senior Security Engineer, iDEFENSE Labs Other Research: nologin.org / uninformed.org

• What is iDEFENSE?

- What is the purpose of this talk?
 - Introduce the core components of a disassembler
 - Refresh binary format parsing concepts
 - Explore programmatic disassembly analysis methods
 - Inspire the audience to take development of binary analysis tools a little further and explore the potential for automated disassembly analysis programs.

Agenda



- Introduction
- Disassember Core Architecture
 - Instruction Decoder
 - IA-32
 - Executable Binary Format Parser
 - Executable and Linkable Format (ELF)
 - Portable Executable (PE)
 - Disassembly Analyzer
- Basic Disassembly Analysis
 - Data Associations
 - Function Recognition
 - Cross-Referencing
 - Hinting
 - System Calls
 - Function Calls
 - Assembly Syntax
 - Demo (codis)

Agenda



- Advanced Disassembly Analysis
 - Path Analysis
 - Loop Detection
 - Data Analysis
 - Static data flow analysis
 - Emulation
 - Data Structure Recognition
 - Demo (ida-x86emu + idastruct)
- Conclusion

Introduction



- Disassemblers decode machine language into human-readable mnemonics
- Reverse-engineering in the software world makes use of a disassembler to understand an unknown or closed system.
- Reverse-engineering has many applications
 - Interoperability
 - Copyright evasion
 - Technology theft
 - Software security

Introduction



- The goal of reverse engineering is to gain a higher understanding of the machine readable code that is available.
- The low-level disassembler is powerful, yet limited. Manual reverse-engineering is tedious.
- Advanced disassemblers are capable of recognizing structures and relationships within binary code.
 - Executable binary format handling
 - Function recognition / argument detection
 - Code and data cross-referencing
 - Structure recognition



Disassembler Core Architecture

Disassembler Core Architecture

- idefense[©]
- The core function of a disassembler is to interpret executable files and decode their instructions.
- The instruction decoder translates compiled binary instructions back into mnemonics as defined by the architecture's reference manuals.
- The executable file parsers are each designed to extract useful information from various executable binary formats.

- DEFENSE[©]
- The IA-32 processor is considered to be a CISC architecture. The instruction set includes many operands which do similar things or combine multiple operations into one instruction.
- RISC architectures have far fewer opcodes and simpler opcode lookup algorithms
- IA-32 has variable length opcodes and opcode extensions, which results in a larger set of tables for opcode and operand decoding.

IA-32 Instruction Decoding



IA-32 Opcode Table and Flags

```
// 1-byte opcodes
INST inst table1[256] = {
                           "add", AM_E|OT_b|P_w,
                                                            AM_G|OT_b|P_r, FLAGS_NONE,
   INSTRUCTION_TYPE_ADD,
                                                                                         1 },
                           "add", AM E OT v P w,
                                                            AM G|OT v|P r, FLAGS NONE,
    INSTRUCTION_TYPE_ADD,
                                                                                         1 },
                           "add", AM G|OT b|P w,
                                                            AM E | OT b | P r, FLAGS NONE,
                                                                                         1 },
  { INSTRUCTION TYPE ADD,
                           "add", AM G|OT v|P w,
                                                            AM_E|OT_v|P_r, FLAGS_NONE,
                                                                                         1 },
  { INSTRUCTION TYPE ADD,
                           "add", AM_REG|REG_EAX|OT_b|P_w, AM_I|OT_b|P_r, FLAGS_NONE,
                                                                                         0 },
   INSTRUCTION TYPE ADD,
                           "add", AM REG REG EAX OT v | P w, AM I OT v | P r, FLAGS NONE,
                                                                                         0 },
   INSTRUCTION TYPE ADD,
   INSTRUCTION TYPE PUSH, "push", AM REG REG ES F r P r,
                                                                                         0 },
                                                            FLAGS_NONE,
                                                                           FLAGS NONE,
                           "pop", AM REG REG ES F r P w,
    INSTRUCTION TYPE POP,
                                                            FLAGS NONE,
                                                                           FLAGS NONE,
                                                                                         0 },
                                  AM_E|OT_b|P_w,
                                                            AM_G|OT_b|P_r, FLAGS_NONE,
    INSTRUCTION_TYPE_OR,
                           "or",
                                                                                         1 },
                                  AM E OT v P w,
                                                            AM G|OT v|P r, FLAGS NONE,
                           "or",
                                                                                         1 },
    INSTRUCTION_TYPE_OR,
// Operand Addressing Methods, from the Intel manual
#define MASK AM(x) ((x) & 0x00ff0000)
                                // Direct address with segment prefix
#define AM A 0x00010000
#define AM_C 0x00020000
                                // MODRM reg field defines control register
#define AM D 0x00030000
                                // MODRM reg field defines debug register
#define AM_E 0x00040000
                                // MODRM byte defines reg/memory address
#define AM G 0x00050000
                                // MODRM byte defines general-purpose reg
. . . .
// Operand Types, from the intel manual
#define MASK_OT(x) ((x) & 0xff000000)
#define OT a 0x01000000
#define OT b 0x02000000
                                // always 1 byte
#define OT c 0x03000000
                                // byte or word, depending on operand
#define OT d 0x04000000
                                // double-word
                                // quad-word
#define OT q 0x05000000
                                // double guad-word
#define OT dq 0x06000000
                                                                 (example taken from from libdasm.h)
```

IA-32 Instruction Decoding

- IA-32 Opcode Decoding
 - Parse opcode prefixes
 - First byte of opcode
 - Indicate multi-byte opcodes or opcode extensions
 - Determine lookup table
 - Perform lookup in opcode table by current index value
- IA-32 Operand Decoding
 - Index opcode table to get operand types and flags
 - Addressing method
 - Register
 - Immediate
 - Displacement
 - Operand type
 - Word
 - Double-word
 - Float

Executable Binary Formats

- idefense[©]
- Executable binary formats instruct an operating system how to initialize the required environment for an executable and how to place the binary in memory for execution.
- The kernel is responsible for:
 - Creating a new task
 - Loading a binary into memory
 - Loading a binary's interpreter
 - Transferring control to the new task
- The kernel understands the binary as a series of memory segments.



- Most binaries are dynamically linked
- Execution control is transferred to the linker rather than the executable's entry point.
- The linker is responsible for:
 - Library loading
 - Symbol relocation
 - Symbol resolution
- The linker interprets the binary as a series of sections with special run-time purposes.

Executable and Linkable Format (ELF)



- Executable and Linkable Format
 - Originally introduced in UNIX SVR4 in 1989 and is now used in Linux and most System V derivatives like Solaris, IRIX, FreeBSD and HP-UX
 - Official reference:

ELF Portable Formats Specification, Version 1.1 Tool Interface Standards (TIS)

 Contains important information for binary analysis including section headers, symbol tables, string tables, dynamic linking information.



- ELF Objects
 - Header info
 - ELF Header
 - Details how to access headers within the object and identifies the executable's properties
 - Section Header Table
 - Details how to access various sections in the file (linker)
 - Program Header Table
 - Details how to load the executable into memory (kernel)
 - Object Code
 - Relocation info
 - Symbols
 - .symtab Contains information about all symbols being defined or imported (not present if binary is stripped)
 - .dynsym Contains information about external symbols that need to be resolved or dynamic symbols that are exported by the binary

• ELF Header

- Located at the beginning of every ELF binary
- Identifies properties of the ELF binary
- Details how to access section and program header tables

```
#define EI NIDENT (16)
typedef struct
 unsigned char e_ident[EI_NIDENT];
                                       /* Magic number and other info */
                                       /* Object file type */
 Elf32 Half
               e type;
                                       /* Architecture */
 Elf32 Half e machine;
                                       /* Object file version */
 Elf32 Word e version;
                                       /* Entry point virtual address */
  Elf32_Addr e_entry;
                                       /* Program header table file offset */
 Elf32 Off
               e phoff;
 Elf32_Off
            e shoff;
                                       /* Section header table file offset */
  Elf32_Word
               e_flags;
                                       /* Processor-specific flags */
  Elf32_Half
               e ehsize;
                                       /* ELF header size in bytes */
 Elf32 Half
               e phentsize;
                                       /* Program header table entry size */
 Elf32 Half
               e phnum;
                                       /* Program header table entry count */
 Elf32_Half
               e_shentsize;
                                       /* Section header table entry size */
                                       /* Section header table entry count */
 Elf32 Half
               e shnum;
 Elf32 Half
               e shstrndx;
                                       /* Section header string table index */
} Elf32 Ehdr;
```

Executable and Linkable Format (ELF)



ELF Section Header Table

– Located by adding:

base_addr + Elf32_Ehdr->e_shoff

- Describes sections in the binary
 - Contains flags that describe memory permissions and type of data contained in the section
 - Can describe relationships between two sections in an ELF file.
- Disassembler should take note of special sections
 - .dynamic, .plt, .got, .symtab, .dynsym, .text

typedef struct		
{		
Elf32_Word	sh_name;	/* Section name (string tbl index) */
Elf32_Word	sh_type;	/* Section type */
Elf32_Word	sh_flags;	/* Section flags */
Elf32_Addr	sh_addr;	/* Section virtual addr at execution */
Elf32_Off	sh_offset;	/* Section file offset */
Elf32_Word	sh_size;	/* Section size in bytes */
Elf32_Word	sh_link;	/* Link to another section */
Elf32_Word	sh_info;	/* Additional section information */
Elf32_Word	sh_addralign;	/* Section alignment */
Elf32_Word	sh_entsize;	/* Entry size if section holds table */
<pre>} Elf32_Shdr;</pre>		



ELF Symbols

- Sections of type SHT_SYMTAB or SHT_DYNSYM contain symbol tables.
 which are identical and can be parsed the same way.
- The st_info member describes symbol type, for example whether the symbol is a code or data object.
- Symbols will be associated with code locations once disassembly is performed.

```
typedef struct
{
   Elf32_Word st_name; /* Symbol name (string tbl index) */
   Elf32_Addr st_value; /* Symbol value */
   Elf32_Word st_size; /* Symbol size */
   unsigned char st_info; /* Symbol type and binding */
   unsigned char st_other; /* Symbol visibility */
   Elf32_Section st_shndx; /* Section index */
} Elf32_Sym;
```

Executable and Linkable Format (ELF)



- ELF Symbol Parsing
 - Enumerate section headers:

- Enumerate the symbol table:

```
for (sym = (base + shdr->sh_offset), symidx = 0;
    symidx < (shdr->sh_size / shdr->sh_entsize);
    sym++, symidx++)
{
    // store symbol information
}
```

- String table lookup:

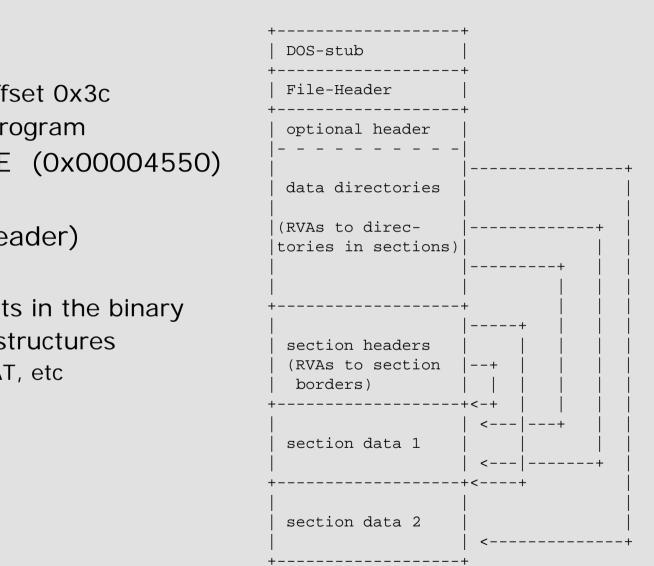
Section	Header	Structure			
typedef	struct				
{					
Elf32_	Word	sh_name;			
Elf32_	Word	sh_type;			
Elf32_	Word	<pre>sh_flags;</pre>			
Elf32_	Addr	sh_addr;			
Elf32_	Off	<pre>sh_offset;</pre>			
Elf32_	_Word	sh_size;			
Elf32_	_Word	sh_link;			
Elf32_	Word	sh_info;			
Elf32_	_Word	sh_addralign;			
Elf32_	_Word	sh_entsize;			
} Elf32_	_Shdr;				
Symbol Table Structure					
typedef	struct				

```
Elf32_Word st_name;
Elf32_Addr st_value;
Elf32_Word st_size;
unsigned char st_info;
unsigned char st_other;
Elf32_Section st_shndx;
Elf32_Sym;
```



- Portable Executable and Common Object File Format
 - Originally introduced as part of the Win32 specification
 - Derived from DEC's Common Object File Format (COFF)
 - Object files are generated as COFF and later linked as PE binaries
 - Offical reference:

Microsoft Portable Executable and Common Object File Format Specification Microsoft Corporation Revision 6.0 - February 1999



DOS Stub + Signature

PECOFF Structure

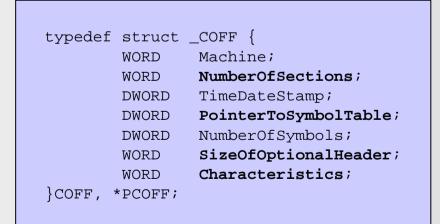
- Pointer to PE Sig at offset 0x3c
- Executable MS-DOS program
- IMAGE_NT_SIGNATURE (0x00004550)
- File Header (COFF)
- Optional Header (PE Header)
- Data Directories
 - Located at static offsets in the binary
 - Point to specific data structures
 - Imports, Exports, IAT, etc
- Section Headers
- Sections





COFF File Header

- Locate by adding the value at offset 0x3c to the base address
- Number of sections
- COFF Symbol table information
- Optional header size
- Characteristic flags
 - Byte ordering
 - Word size



+ DOS-stub	+
File-Header	+
optional header 	+
 data directories	
 (RVAs to direc- tories in sections) 	 + +
 section headers (RVAs to section borders) +	+ + -++
 section data 1 +	< + < +
 section data 2 +	 <+ +



• Optional Header (PE Hdr)

typedef	struct _	_OPTHEADERS{				
	WORD	Magic;				
	BYTE	MajorLinkerVersion;				
	BYTE	MinorLinkerVersion;				
	DWORD	SizeOfCode;	11	code	segment	size
	DWORD	SizeOfInitializedData;	11	data	segment	size
	DWORD	SizeofUninitializedData;	11	data	segment	size
	DWORD	AddressOfEntryPoint;	11	entry	y point	
	DWORD	BaseOfCode;				
	DWORD	BaseOfData;				
	DWORD	ImageBase;				
	DWORD	SectionAlignment;				
	DWORD	FileAlignment;				
	WORD	MajorOperatingSystemVersion;				
	WORD	MinorOperatingSystemVersion;				
	WORD	MajorSubsystemVersion;				
	WORD	MinorSubsystemVersion;				
	DWORD	Reserved;				
	DWORD	SizeOfImage;				
	DWORD	SizeOfHeaders;				
	DWORD	CheckSum;				
	WORD	Subsystem;				
	DWORD	DllCharacteristics;				
	DWORD	SizeOfStackReserve;				
	DWORD	SizeOfStackCommit;				
	DWORD	SizeOfHeapReserve;				
	DWORD	SizeOfHeapCommit;				
	DWORD	LoaderFlags;				
	DWORD	NumberOfRvaAndSizes;	11	data	director	ies
}OPTHEAI	DERS, *PC)PTHEADERS;				



COFF Section Tables

– Located by adding:

```
base_addr + *(uint32)(base_addr + 0x3c)
+ sizeof(COFF) + PCOFF->SizeOfOptionalHeader
```

- Then enumerate the data directories until you hit the section tables
- Relocation entries are only present in object files
- Line-number entries associate code with line numbers in source files
- Characteristic flags indicate section types, memory permissions, and alignment information

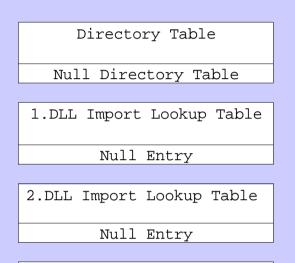
typedef struct	_SECTIONTABLES {	
BYTE	Name[8];	// Section name
DWORD	VirtualSize;	<pre>// Size of section in memory</pre>
DWORD	VirtualAddress;	<pre>// Address of mapped section</pre>
DWORD	SizeOfRawData;	// Size of section on disk
DWORD	PointerToRawData;	// Section file offset
DWORD	PointerToRelocations;	<pre>// Relocation entries file offset</pre>
DWORD	PointerToLineNumbers;	// Line-number entries file offset
WORD	NumberOfRelocations;	// Number of relocation entries
WORD	NumberOfLineNumbers;	// Number of line-number entries
DWORD	Characteristics;	<pre>// Characteristics flags</pre>
}SECTIONTABLES,	*PSECTIONTABLES;	



PECOFF Symbols

- Data_Directory[1] Import Directory
 - .idata section
- Import Directory entries describe DLLs
 - DLL Name
 - RVA of Import Lookup Table
 - RVA of Import Address Table
- Image Thunk Data
 - Table of structures describing functions to be imported from the module

typedef	<pre>struct _IMAGE_IMPORT_DESCRIPTOR {</pre>			
	union {			
		DWORD Characteristics;		
		<pre>PIMAGE_THUNK_DATA OriginalFirstThunk;</pre>		
	} DUMMYUNIONNAME;			
	DWORD	TimeDateStamp;		
	DWORD	ForwarderChain;		
	DWORD	Name;		
	PIMAGE_	THUNK_DATA FirstThunk;		
} IMAGE_	_IMPORT_I	DESCRIPTOR, *PIMAGE_IMPORT_DESCRIPTOR;		



Hint Name 7	Table
-------------	-------



- PE Symbol Parsing
 - Locate and loop Import Directory Table
 - Get the pointer to the FirstThunk

IDD->FirstThunk

Loop Thunks for symbol import data

struct IMAGE_IMPORT_BY_NAME[]

```
Import name entry
typedef struct IMAGE IMPORT BY NAME {
        WORD
                Hint;
        BYTE
                Name[1];
 IMAGE IMPORT BY NAME, * PIMAGE IMPORT BY NAME;
Import Thunk
typedef struct _IMAGE_THUNK_DATA {
        union {
                          ForwarderString;
                LPBYTE
                PDWORD
                          Function;
                          Ordinal;
                DWORD
                PIMAGE IMPORT BY NAME
                                       AddressOfData;
        } u1;
 IMAGE_THUNK_DATA, *PIMAGE_THUNK_DATA;
```

Directory Table
Directory rabie
Null Dimentany Mable
Null Directory Table

1.DLL Import Lookup Table

Null Entry

2.DLL Import Lookup Table

Null Entry

Hint Name Table



- The final component of a useful disassembler for reverse engineering is the disassembly analyzer.
- The analyzer builds a database of associations from the binary and can perform additional specialized disassembly analysis tasks.
- Disassembly analyzers attempt to aid the reverse engineer by automating some of the manual processes used when looking at assembly code dead listings.
- Programmatic disassembly analysis is an imperfect science. The more powerful the analyzer becomes, the closer it becomes to truly emulating the disassembled code



Disassembly Analysis



- A wealth of information can be generated using very simple analysis logic.
- Data associations including function detection, static data references, string references, and execution branch references can be performed through simple opcode and operand parsing.
- Assembly hinting or commenting can aid the reverse-engineer by eliminating guesswork.
 - System call detection and argument labelling
 - Function call calling convention and argument detection
 - Assembly syntax hints



Function detection

- Standard function detection is done by pattern matching for function prologues.
- Prologues are generated during compilation and typically perform tasks including frame initialization and stack canary generation.

Standard function prologue	
55 push %ebp	; push old frame pointer
89 e5 mov %esp, %ebp	; store current stack pointer as new frame

Migrogoft Vigua	l Studio "hotfix" function prologue for system libraries and drivers
MICIOSOIC VISUA	I Studio mottix function protogue for system libraries and drivers
90	nop ; five nops make space for a long relative jmp
90	nop ;
	; Begin Function Prologue
8b ff	mov %edi, %edi ; 2-byte nop (space for short relative jmp)
55	push %ebp ; push old frame pointer
89 e5	mov %esp, %ebp ; store current stack pointer as new frame



- Function detection without prologue
 - Cross reference calls in case of -fomit-frame-pointer

 080483b4					
	; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;				
	;;; S U B R O U T I N E ;;;				
	, , , , , , , , , , , , , , , , , , , ,				
	sub_08048	33b4:	;	xrefs:	0x08048403
	sub	\$0x3c, %esp	;		
080483b7	mov	0x40(%esp), %eax	;		
080483bb	mov	<pre>%eax, 0x4(%esp)</pre>	;		
080483bf	lea	0x10(%esp), %eax	i		
080483£4	shr	\$0x4, %eax	;		
		• •	,		
080483f7	shl	\$0x4, %eax	;		
080483fa	sub	%eax, %esp	i		
080483fc	movl	\$0x804851e, (%esp)	;		
 08048403	call	0x80483b4	;		

 Symbolic function names are created for code locations that do not have a pre-defined symbol associated with them.



Cross Referencing

- Disassembly analyzers create a database of cross-references which describe the relationships between code and data in the binary.
- Cross-references are determined by examining immediate operand values or by tracing register exchanges to watch references to a known value.
- The use of an instruction decoder core which implements operand permissions flags is required.
 - libdasm available at nologin.org by jt
 - libdisasm available at bastard.sf.net by _mammon
- For each instruction, analyze the operands for internal relationships
 - Check for operand types: IMMEDIATE, MEMORY, REGISTER
 - Check operand permission flags
- Cross-references are stored in data-structures for later use.



 Code execution flow can be determined by detecting code branches which are indicated by the RET, IRET, INT, CALL and the various JMP opcodes for IA-32.

Flow Control Instructions

- Call
 - Indicates a new function
 - Needs to be checked against symbol tables when displaying disassembly
 - Pushes calling address before transferring execution control
- Branch
 - Any opcode of the JMP variety
 - Indicates new code 'block'
 - Code blocks can be analyzed for functionality
 - Used for loops, signal handlers, etc
- Return
 - Used to divert flow control by popping a pointer from the stack



 Symbols, strings, and pointers within pre-initialized data sections in the binary are examples of data cross-references that can be determined through simple disassembly analysis.

[00401050			
	00401050			
	•••••	;;;;;;;;;	* ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;	
	· · · · · · · ·	;;; S U E	BROUTINE;;;	
		;;;;;;;;;;	* ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;	
		sub_00401	L050:	; xrefs: 0x004010a7
		push	%ebp	;
	00401051	mov	%esp, %ebp	;
	00401053	sub	\$0x8, %esp	;
	00401056	movl	\$0x402000, (%esp)	; "this string is a pre-initialized variable\n"
	0040105d	call	<printf></printf>	; imported shared library symbol
	00401062	leave		;
	00401063	ret		;
•	004010a7	call	<sub_00401050></sub_00401050>	; symbolic function names cross-referenced
	004010ac	mov	\$0x0, %eax	;
	004010b1	leave		;

Hinting



- Disassemblers should use a database of information regarding system calls and standard system library calls to aid in disassembly hinting.
- System Call hinting can help a reverse engineer determine what system services a function utilizes.
 - Syscall Numbers are stored in /usr/src/linux/include/asm/unistd.h
 - Arguments are typically passed in registers, so once data xrefs are applied we can tell if user-supplied data is being used in a system call.
- Function argument types and high level datastructures can be parsed from header files.
 - Every platform has a set of default libraries and headers.
 - The more the disassembler knows about variable types, the better it can understand how the data is being used.

Hinting



- Function call argument detection
 - Function prologues swap the the current stack pointer into ebp to represent the base of the stack for the local function
 - Function arguments can be determined by internal references to offsets of ebp
 - In the case of code compiled without frame pointers, offsets to esp will be used.
 - Arguments can be determined as local variables vs passed arguments depending on their offset to ebp
 - Depending on calling convention, arguments to functions are typically passed via the stack
 - Stdcall push args in reverse order to the stack (last to first)
 - Fastcall uses registers when possible to hold args
 - Argument types can be determined via basic heuristics or by prototype parsing
 - Heuristics can determine if passed values are pointers to memory, string references or integer values



- The features described in this section should be standard fare.
- IDA Pro, HTE, the bastard, and Codis are currently the only disassemblers available which implement most of the features.
- Required development time: 2 3 weeks

Codis Demo



Advanced Disassembly Analysis

Advanced Disassembly Analysis



- The flexibility offered by DataRescue's IDA Pro SDK has allowed for recent advancements in disassembly analysis capabilities.
- IDA Pro plug-ins have access to the program's internal database which allows for rapid development of concept ideas.
 - Path Analysis
 - Peter Silberman's loop detection plugin
 - Data Analysis
 - idastruct data structure enumeration



- Path analyzers recursively follow execution flow to build a control flow graph.
- When reverse engineering, entire code paths can be quickly grouped for functionality to speed the code recognition process.
- Linear disassemblers can not determine the relationships of code blocks, and may disassemble instructions incorrectly if data is injected in-between compiled code

Path Analysis



 Hand written assembly code can cause disassemblers to generate code listings that are completely incorrect:

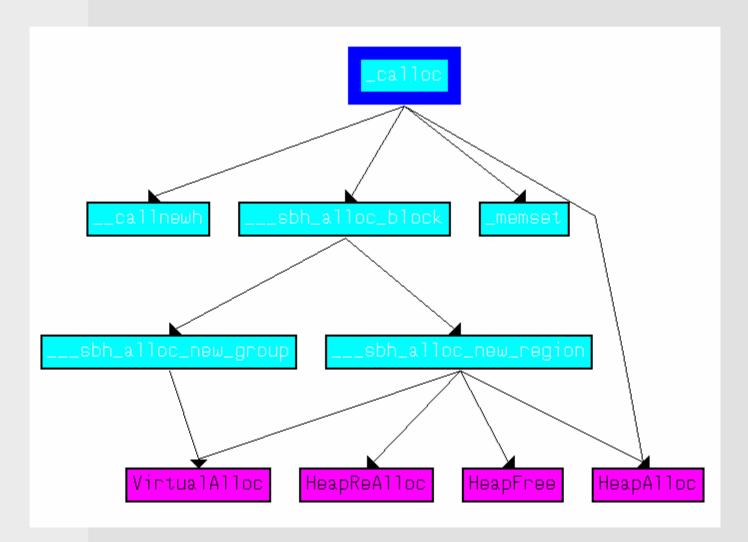
```
(gdb) disas loc
Dump of assembler code for function loc:
0x0040107a <loc+0>:
                        pushw $0xfeeb
0x0040107e <loc+4>:
                               0x40107c <loc+2>
                        jmp
                        pushl 0xaabbccdd
0x00401080 <loc+6>:
                               $0x0,%eax
0x00401086 <loc+12>:
                        mov
0x0040108b <loc+17>:
                        leave
0x0040108c <loc+18>:
                        ret
```

```
Breakpoint 1, 0x0040107a in loc ()
1: x/i $pc 0x40107a <loc>: pushw $0xfeeb
(gdb) si
0x0040107e in loc ()
1: x/i $pc 0x40107e <loc+4>: jmp 0x40107c <loc+2>
(gdb) si
0x0040107c in loc ()
1: x/i $pc 0x40107c <loc+2>: jmp 0x40107c <loc+2>
...
```

Path Analysis



 Once a control flow graph has been built programmatically, it can easily be represented using data visualization software.





- Loop detection is an advanced application of control flow analysis.
- Loop detection can be applied to recognize program structure as well as specific types of vulnerabilities.
- Recognizing loops can aid other disassembly analysis tasks and eliminate heavy analysis of code multiple times.
- Example: Peter Silberman's Loop Detection Plugin
 - Designed to help reverse-engineers locate code loops that may lead to exploitable scenarios.

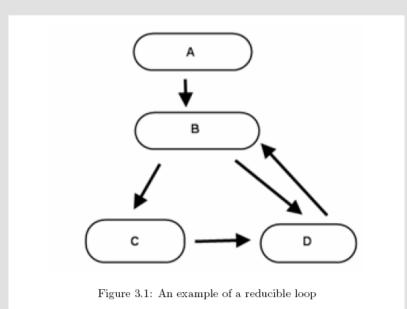


- Reducible loops have one entry point and can be reduced to a Natural Loop.
- Natural Loop structure is found by determining node dominance in the control flow graph.
- If node C is unreachable other than through node B, then B dominates node C.

In this diagram, there is a small loop between B and D.

The *Natural Loop* can be determined by locating the path between the two nodes that are under dominance of B.

The secondary loop between B and D can be ignored when determining the *Natural Loop*



Loop Detection



- Traditional loop detection algorithms are known to have trouble detecting loops with more than one potential entry point (non-reducible loops).
- Using IDA's powerful cross-referencing and flow control graphing algorithms, Peter has developed a method for identifying irreducible loops.
- Peter's work can be found on www.uninformed.org

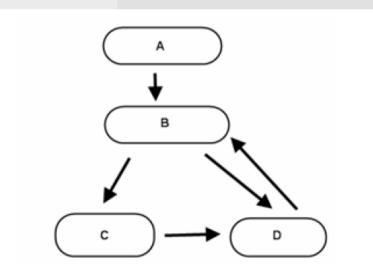


Figure 3.1: An example of a reducible loop

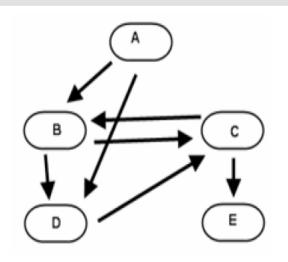
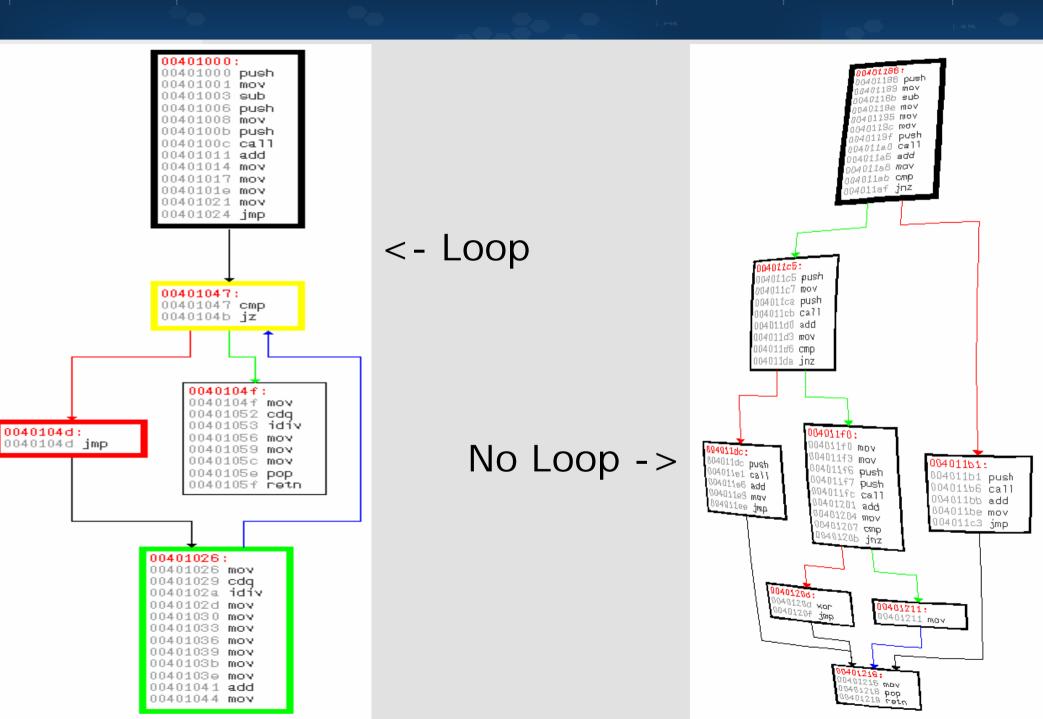


Figure 3.2: An example of an irreducible loop

Loop Detection







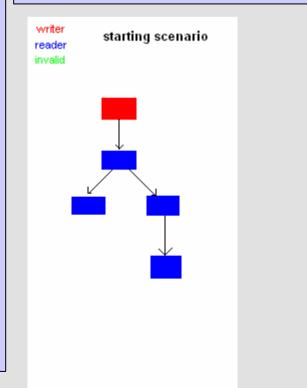
- Unlike code paths, analyzing data relationships is a non-trivial exercise.
- Data references are occasionally supplied as immediate values, but are more often passed around in registers to perform operations.
- There are numerous obstacles to overcome when tracing assembly for the purpose of data reference tracking – it has yet to be implemented successfully.
- To follow data paths, a variable tracing algorithm must be developed... or does it?



Variable Tracing

```
// init trace
add xref(ea, dst);
// simplified variable tracing loop
while(ea = ea.next)
   while(op = operand.next)
      mask = SIZE_MASKS[opsize];
      switch(op->type)
      case o imm:
         val = op->addr & mask;
         break;
      case o displ:
         val = (registers[op->reg] + op->addr)& mask;
         break;
      case o_phrase:
         val = registers[op->phrase] & mask;
         break;
if(search_itrace_list(val))
   remove xref(ea, dst);
else if search itrace list(src)
   add_xref(ea, dst);
```

```
unsigned long registers[8];
unsigned long eip;
unsigned long eflags;
typedef struct _itrace {
    struct _itrace *next, *prev;
    ea_t addr; // address of reference
    ea_t xref; // address referenced
    unsigned char reftype; // RWX
} itrace_t;
```





Variable Tracing

```
// init trace
add xref(ea, dst);
// simplified variable tracing loop
while(ea = ea.next)
   while(op = operand.next)
      mask = SIZE_MASKS[opsize];
      switch(op->type)
      case o imm:
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         break;
      case o displ:
         val = (registers[op->reg] + op->addr)& mask;
         break;
      case o_phrase:
         val = registers[op->phrase] & mask;
         break;
if(search_itrace_list(val))
   remove xref(ea, dst);
else if search itrace list(src)
   add_xref(ea, dst);
```

```
unsigned long registers[8];
unsigned long eip;
unsigned long eflags;
typedef struct _itrace {
          struct itrace *next, *prev;
          ea t addr; // address of reference
          ea t xref; // address referenced
          unsigned char reftype; // RWX
  itrace t;
writer
                               scenario #1
        starting scenario
reader
invalid.
                                  write occurs at addr
                                  referenced by this node
                                    invalidate node ref to
                                    node derived from
```



Variable Tracing

```
// init trace
add xref(ea, dst);
// simplified variable tracing loop
while(ea = ea.next)
   while(op = op.next)
      mask = SIZE_MASKS[opsize];
      switch(op->type)
      case o imm:
         val = op->addr & mask;
         break;
      case o displ:
         val = (registers[op->reg] + op->addr)& mask;
         break;
      case o_phrase:
         val = registers[op->phrase] & mask;
         break;
if(search_itrace_list(val))
   remove xref(ea, dst);
else if search itrace list(src)
   add_xref(ea, dst);
```

```
unsigned long registers[8];
unsigned long eip;
unsigned long eflags;
typedef struct _itrace {
          struct itrace *next, *prev;
          ea t addr; // address of reference
          ea t xref; // address referenced
          unsigned char reftype; // RWX
  itrace t;
writer
                             scenario #2
        starting scenario
reader
                                write occurs at addr
invalid.
                                referenced by this node
```



Combinatorial Explosion

- Occurs when a huge number of possible combinations are created by increasing the number of entities which can be combined--forcing us to consider a constrained set of possibilities when we consider related problems.
- Variable tracing is susceptible to combinatorial explosion and infinite recursion if bounds are not set on the depth of the search.
- In theory static data reference tracing is possible but has yet to be successfully implemented beyond proof of concept.

Emulation



- CPU emulation can be used as a powerful resource when analyzing static code.
- CPU Emulation involves the execution of instructions in a virtual CPU.
- Virtual CPUs emulate the core components of a hardware CPU in software.
 - Instruction decoding/evaluation
 - Registers
 - Memory
- Emulation is "safe"
 - depending on implementation of course

ida-x86emu



- ida-x86emu is an opensource emulator written by Chris Eagle and Jeremey Cooper
 - Emulator codebase can be easily hooked for special analysis purposes.
 - Undergoing development
 - Some features are missing but code is easily hackable
 - Use the CVS version!
- Evaluates complex instruction sequences
- Emulates dynamic memory allocator functionality
- Can hook PE imports and load required libraries
 Sometimes has some hiccups currently looking into this



- idastruct is data structure reference tracing code built on top of ida-x86emu.
- Arbitrary bounds within the emulated memory space can be traced using simple logic.
- As operands are evaluated for each instruction, a check is made to determine if that operand is referencing memory that is being traced.
- IDA database is updated with structure information and member data as references are detected and types are applied to the reference.

idastruct



Structure reference tracing

```
void struct_trace(ea_t addr)
   strace_t *trace;
   ua_ana0(addr);
   for(int opnum = 0; cmd.Operands[opnum].type != o_void; opnum++)
      op_t *op = &cmd.Operands[opnum];
      // evaluate operand value
      for(trace = strace; trace; trace = trace->next)
         // determine if operand value points within trace bounds
         if(val >= trace->base && val <= trace->base + trace->size)
            struc_t *sptr = trace->sptr;
            member t *mptr = get member(sptr, val - trace->base);
            if(!mptr)
               char *mtype;
               switch(get_dtyp_size(op->dtyp))
               ...
               // assign a name to the new member that indicates type size
```

idastruct



Structure reference tracing

```
void struct trace(ea t addr)
       // create ida structure member
       if(struct member add(sptr, name, val - trace->base, 0, NULL,
                                qet dtvp size(op->dtvp)) < 0)</pre>
           trace = trace->next;
           continue;
       mptr = get_member(sptr, val - trace->base);
   // update member reference
                                      .text:00401037 010
                                                                         mov
                                                                                 edx, [ebp+arg 0]
                                      .text:0040103A 010
                                                                         mov
                                                                                 eax, dword ptr [edx+struct_0._dword_8]
   tid t path[2];
                                      .text:0040103D 010
                                                                         push
                                                                                 eax
   path[0] = sptr->id;
                                      .text:0040103E 014
                                                                         mov
                                                                                 ecx, [ebp+var 4]
                                      .text:00401041 014
   path[1] = mptr->id;
                                                                         push
                                                                                 ecx
                                      .text:00401042 018
                                                                         MOV
                                                                                 edx, [ebp+arg 0]
   op_stroff(addr, opnum,
                                                                                 eax, word ptr [edx+struct 0. word 12]
                                      .text:00401045 018
                                                                         MOVSX
               path, 2, 0);
                                      .text:00401049 018
                                                                         push
                                                                                 eax.
                                                                                 offset str->DDDD ; "%d %d %d %d"
                                      .text:0040104A 01C
                                                                         push
                                      .text:0040104F 020
                                                                         call
                                                                                 printf
                                      .text:0040104F
                                      .text:00401054 020
                                                                         add
                                                                                 esp, 14h
                                      .text:00401057 00C
                                                                                 ecx, [ebp+arg 0]
                                                                         MOV
                                      .text:0040105A 00C
                                                                                 word ptr [ecx+struct 0. word 12], 4D2h
                                                                         mov
                                      .text:00401060 00C
                                                                                 [ebp+var 4], 7Bh
                                                                         mov
                                      .text:00401067 00C
                                                                                 edx, [ebp+arg 0]
                                                                         MOV
                                      .text:0040106A 00C
                                                                         MOV
                                                                                 eax, dword ptr [edx+struct 0. dword 0]
                                      .text:0040106C 00C
                                                                         MOV
                                                                                 ecx, [ebp+var 4]
                                      .text:0040106F 00C
                                                                                 dword ptr [eax+struct 1. dword 0], ecx
                                                                         MOV
                                      .text:00401071 00C
                                                                                 edx, [ebp+arg 0]
                                                                         MOV
                                                                                 eax, dword ptr [edx+struct 0. dword 0]
                                      .text:00401074 00C
                                                                         mov
```

Conclusion



- The ability to identify arbitrary structures via binary analysis should speed software reversing in all areas.
- Directly applies to vulnerability discovery through automation of fuzz template generation.
- Further analysis may be performed on the structure relationships within execution paths to tie complete structure hierarchies together.



Questions?